

Universal High Brightness LED Driver

- REVISION 2 -

INTRODUCTION

DESCRIPTION

The MN9910B is a dimmable current-mode constant current LED driver IC. It drives an external MOSFET to accurately regulate the current in the LED string. The MOSFET can be sized for all types of LEDs including Power LEDs beyond 1W. Its robust 450V rating makes it universally applicable to systems powered directly from Mains sources or from popular PFC sources. Its low voltage rating of 8V makes it suitable as well for low/medium voltage sources. The internal linear regulator generates 7.5V_{Vdd}, which is also made available for external use, thus saving the cost of an external regulator. The MN9910 also draws less standby current than competitive devices.

Current dimming can be achieved through the 0 - 250mV linear dimming port LD, or else by PWM methods on the PWMD port with a duty ratio of 0 - 100% and a frequency of up to a few kilohertz.

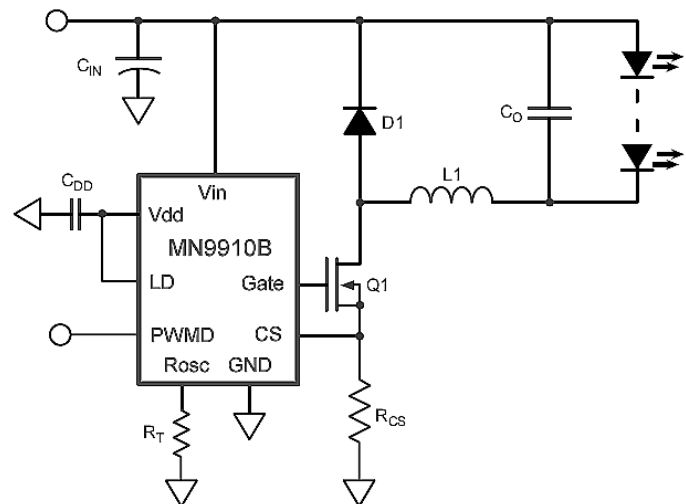
The MN9910B is ideally suited for buck LED drivers. Since it operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation.

The MN9910B is an ideal and affordable driver for low cost LED string control solutions, requiring only three external components (apart from the power stage).

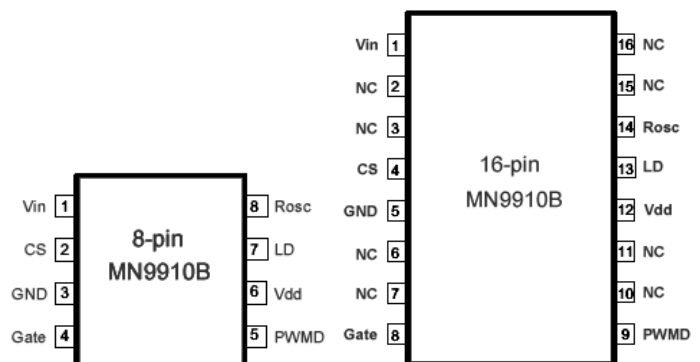
FEATURES

- Affordable and high-efficiency LED driver
- Form and fit compatible with market solutions
- Open loop peak current controller
- Internal 8.0 to 450V linear regulator
- Constant frequency /constant off-time operation
- 0- 250 mV linear dimming and
- 0 - 100% PWM dimming
- Requires few external components

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION



APPLICATIONS

- Lighting, recessed lighting, street lighting
- Signage and decorative lighting
- RGB backlighting, flat panel backlighting
- LED control powered by the Mains
- AC/DC and DC/DC LED driver applications
- General purpose constant current source
- Chargers

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING		
Parameter	Rating	Unit
Vin to GND	-0.5 to +480	V
Vdd to GND	12	V
CS, LD, PWMD, Gate, R _{OSC} to GND	-0.3 to (Vin + 0.3)	V
Storage Temperature Range	-65 to +150	°C
Junction Temperature Range	-40 to +150	°C
Lead Temperature	300	°C
Continuous Power Dissipation (T _A = +25°C): - 8-pin SOIC - 16-pin SOIC	630 1300	mW

Thermal Resistance		
Package	θ _{ja}	Unit
8-pin SOIC	128	°C/W
16-pin SOIC	82	°C/W

OPERATING CHARACTERISTICS

PARAMETER	TEST CONDITIONS	PARAMETERS			UNITS
		MIN.	TYP.	MAX.	
	<i>T_A = 25°C and VIN = 12V, unless otherwise noted.</i>				
INPUT					
V _{inDC} , Input DC supply voltage range (1) (3)	DC input voltage	8	-	460	V
I _{inSD} , Shut-down mode supply current (3)	Pin PWMD to GND	-	0.3	0.6	mA
INTERNAL REGULATOR					
V _{dd} , Internally regulated voltage	Vin= 8V, I _{dd_ext(2)} = 0, 500pF at Gate; RT = 226kΩ, PWMD = Vdd	7.4	7.6	7.8	V
ΔV _{dd, line} , Line regulation	Vin= 8V – 450V, I _{dd_ext(2)} = 0, 500pF at Gate; R _{OSC} = 226kΩ, PWMD = Vdd	0	-	0.5	V
ΔV _{dd, load} , Loaded Regulation	I _{dd_ext(2)} = 0 - 1mA, 500pF at Gate; R _{OSC} = 226kΩ, PWMD = Vdd	0	-	180	mV

INTERNAL REGULATOR (cont.)

UVLO, Vdd undervoltage lockout threshold (3)	V_{dd} rising	6.45	6.70	6.95	V_{in}=8V
ΔUVLO, Vdd undervoltage lockout hysteresis	V_{dd} falling	350	500	640	mV
I_{in,max}, current that the regulator can supply before IC goes into UVLO (4)	V_{in}=8V	5.0	-	-	mA

PWM DIMMING

V_{EN(low)}, Pin PWM input low voltage (3)	V_{in}=8 – 450V	-	1.4	0.80	V
V_{EN(high)}, Pin PWM input high voltage (3)	V_{in}=8 – 450V	2	1.4	-	V
R_{EN}, Pin PWM Pull-down resistance	V_{PWM}=5V	50	100	150	KΩ

CURRENT SENSE COMPARATOR

V_{CS,TH}, Current sense pull-in threshold voltage	-40°C < T_A < +85°C T_A < +125°C	225 213	250 250	275 287	mV mV
V_{OFFSET}, Offset voltage for LD comparator (3)		-16	-	16	mV
T_{BLANK}, Current sense blanking interval (3)	V_{LD} = V_{dd}, V_{CS} = V_{CS,TH} + 50mV after T_{BLANK}	150	250	280	ns
T_{DELAY}, Delay to output	V_{LD} = V_{dd}, V_{CS} = V_{CS,TH} + 50mV after T_{BLANK}	-	70	110	ns

OSCILLATOR

f_{OSC}, Oscillator frequency	R_T=1MΩ R_T=226KΩ	20 80	25 100	30 120	KHz KHz
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GATE DRIVER

I_{SOURCE}, Gate sourcing current	V_{Gate} = 0V, V_{dd} = 7.5V	36	-	-	mA
I_{SINK}, Gate sinking current	V_{Gate} = V_{dd}, V_{dd} = 7.5V	230	-	-	mA
T_{RISE}, Gate output rise time	C_{Gate} = 500pF, V_{dd} = 7.5V	-	167	194	ns
T_{FALL}, Gate output fall time	C_{Gate} = 500pF, V_{dd} = 7.5V	-	22	28	ns

(1) Also limited by package power dissipation limit, whichever is lower.

(2) V_{dd} load current external to the MN9910B.

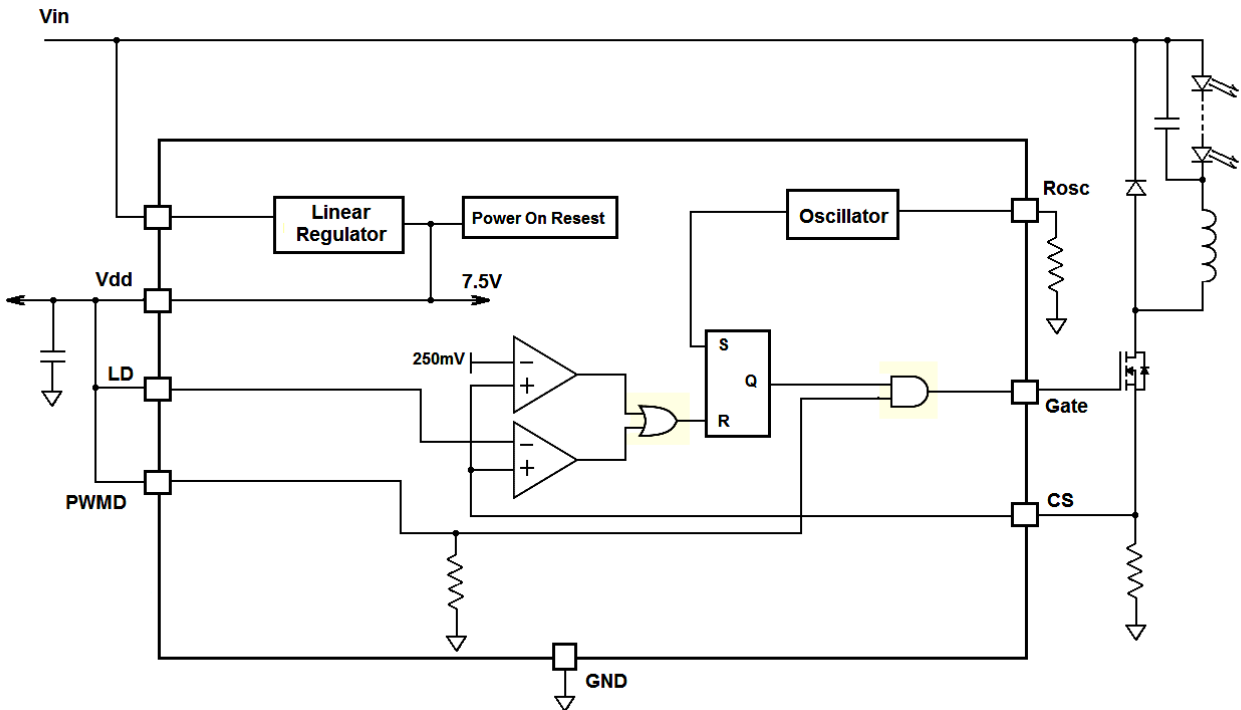
(3) Denotes the specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C.

(4) Guaranteed by design.

PIN DESCRIPTION

8-pin SOIC	16-pin SOIC	Name	Description
1	1	Vin	V-Input. Main power for the LED Driver system. It is the input for the High Voltage tolerant Linear Regulator
2	4	CS	Current Sense. Used to sense current peaks in the inductor, through a sense resistor to GND. Nominally, the current sensors will trip when the voltage at CS is 250mV, or else the Linear dimming value, if it is lower.
3	5	GND	Return point for all circuitry. This must be anchored to the lowest available potential in the system.
4	8	Gate	Gate. Drive to the external Power MOSFET
5	9	PWMD	Pulse Width Modulation Dimming. PWM diming can be performed through this pin. Should be driven with square waves in the low kHz. A logic low input here will turn off the MOSFET driver. If this pin is tied to Vdd, PWMD is not operative.
6	12	Vdd	Vdd. This internally-regulated DC voltage can provide up to 5mA for external circuitry.
7	13	LD	Linear Dimming. For input voltages less than 250mV, this can be used to linearly adjust the LED brightness. If tied to Vdd, then Linear Dimming is not operative.
8	14	Rosc	A resistor from here to GND sets the oscillator frequency. From here to Gate sets Constant off-time.
-	2, 3, 6, 7, 10, 11, 15, 16	N/C	No Connect

BLOCK DIAGRAM AND TYPICAL APPLICATION



1. ORDERING INFORMATION

MN9910B"T"- "P"-TR

"T" for temperature= "C" for commercial (0 - 70°C) or "I" for industrial (-20°C - +85°C) - Default or no indication means "C"

"P" for packaging= "SO8" or "SO16"

"TR" for Tape and Reel - No indication means delivery in tube (for SOIC only)

2. APPLICATION INFORMATION

The MN9910B is a buck LED driver using open-loop peak current mode control. Accurate LED current control is achieved by means of a low-side sense resistance, eliminating high side current sensing and the design of any closed loop compensation. The MN9910 requires a minimum of external components and allows dimming of the LED current with both Linear and PWM methods.

For constant-frequency operation, a resistor connected from the R_{OSC} pin to ground programs the frequency of operation. (Constant off-time is described below). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the MN9910B which causes the Gate driver to turn on. A blanking circuit inhibits the reset input of the SR flip flop and prevents false turn-offs due to the turn-on spike. Even with this blanking feature, a small filter between the sense resistor and the CS pin is recommended (RC ~ 100ns). When the MOSFET is turned on, the Inductor current begins ramping up. This current flows through the external sense resistor RCS and produces a ramp voltage at the CS pin. The comparators compare the CS pin voltage to both the voltage at the LD pin and the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the Gate output goes low. The Gate goes low until the SR flip flop is set by the oscillator. Allowing a 30% ripple in the inductor, the current sense resistor RCS can be set using:

$$RCS = 0.25V / (1.15 * I_{LED}(A))$$

Or

$$RCS = VLD / (1.15 * I_{LED}(A))$$

VLD will dominate the RCS calculation if it is less than 250mV. In practical applications, one might purposely set RCS a little low, so that adjustments on the VLD pin can either trim or dim the output.

At duty cycles greater than 50%, the Constant Frequency peak current mode control scheme goes into subharmonic oscillations. To prevent this, an artificial slope can be added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form, due to the added

delay. A constant off-time peak current control scheme can easily operate at duty cycles greater than 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, constant off-time operation will lead to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. MN9910B can be configured for either of the two modes of operation by changing the connection of the Rosc Resistor (see Oscillator, section 5).

3. INPUT VOLTAGE REGULATOR

The MN9910B contains a novel high-voltage linear regulator operating directly from its VIN pin, rated from 8.0 - 460VDC. When this voltage range is applied at the VIN pin, the MN9910B maintains a regulated 7.5V at the VDD pin. This voltage is used to power the IC and any external circuitry needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor (2.2uF, typical) to provide regulation during high frequency current spikes required by the GATE driver.

As the VIN voltage becomes higher in practice, any current drawn by external loads on Vdd add to the internal current requirements. Their sum is multiplied by the VIN value to infer more power dissipation for the MN9910B. Thus, operation at the full rated Voltage is not recommended for high temperature applications.

Example: If a 16-pin SOIC (junction to ambient thermal resistance $R_{\theta,j-a} = 82^{\circ}\text{C/W}$) MN9910B draws about $I_{IN} = 3.0\text{mA}$ from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about $\Delta T = 100^{\circ}\text{C}$, the maximum voltage at the VIN pin would be:

$$\begin{aligned} VIN(\text{max}) &= \Delta T / (R_{\theta JA} * I_{in}) \\ VIN(\text{max}) &= 100C / (82 * 3\text{mA}) \\ VIN(\text{max}) &= 406.5V \end{aligned}$$

In these cases, to operate the MN9910B from higher input voltages, a Zener diode can be added in series with the VIN pin to absorb some of the power from the MN9910B. In the above example, using a 51V zener diode will allow the circuit to work up to 450V.

The input current drawn from the VIN pin is a sum of the 0.6mA(max) current drawn by the internal circuit, external loads on Vdd, and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external FET).

$$I_{IN} \cong 0.6\text{mA} + I_{dd}(\text{ext_load}) + Q_{Gate} * fS$$

In the above equation, fS is the switching frequency and Q_{Gate} is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

The MN9910B can also be operated by applying a supply voltage at the VDD pin greater than the internally regulated 7.5V (12V max allowed). This turns off the internal regulator and the IC will operate directly off the voltage supplied at the VDD pin. This will also relieve the power dissipation of the MN9910, described above.

4. CURRENT SENSE

Referring to the block diagram: The current sense input of the MN9910B goes to the noninverting inputs of two comparators, which both have the ability to shut-off the GATE through the RS Latch. The comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 150-280ns blanking time which prevents spurious turn-offs of the external FET due to the turn-on spike normally present in peak current mode control. Internal blanking might not be enough to filter out the turn-on spike. In these cases, an external RC filter (RC ~ 100ns) needs to be added between the external sense resistor (RCS) and the CS pin. A proper layout, minimizing external inductance, will prevent false triggering of these high-speed (80ns) comparators.

5. OSCILLATOR

If a resistor is connected from R_{OSC} to GND, the MN9910B operates with constant frequency, with the following equation determining the period:

$$T_{osc}(\mu s) = (R_{osc}(k\Omega) + 22) / 25$$

Example: If R_{osc} is 226k Ω , T_{osc} would be 9.92 μ s, yielding a frequency of about 100kHz.

If the resistor is connected between R_{OSC} and GATE, the MN9910B operates in a constant off-time mode and the above equation yields the off-time.

6. GATE OUTPUT

Care must be taken to select the external MOSFET and oscillation frequency judiciously, as this will impact power dissipation for the MN9910, and for the switching performance of the MOSFET.

As noted in Section 2, part of the power drain on the Vin pin is the product of the Total Gate Charge (available on the MOSFET data sheet), and the frequency of oscillation. For example, a 100kHz time base and a 20nC MOSFET will drain 2mA through the Vin Pin. This gets multiplied directly by the voltage at Vin, to yield additional dissipation for the IC, as covered in Section 2. It is significant that this power dissipation term will be the same regardless of dimming levels if Linear dimming through the VLD pin is performed. However, if dimming is done with PWM techniques on the PWMD pin, then this additional power term will be weighted by the duty cycle of the IC.

Selection of the MOSFET also affects the choice of oscillator frequency, due to the time required for the MOSFET when switching. In general, it is good to keep the transient switching times of the MOSFET to no more than about 10% percent of the pulse width. If a 100kHz oscillation frequency is chosen, and a 25% duty cycle is expected, then the pulse width will be 2.5 μ s. The rise and fall times, combined, may be up to 200ns with reasonable predictability for the output versus linear dimming. At low-light linear dimming levels, the rise/fall times will become a larger fraction of the on-time, requiring better accounting of that effect for predictability and modeling. It must be remembered that the minimum pulse width is about 450ns.

Bench assessment is always best. In practice, connecting MOSFETS with 12nC of Total Gate Capacitance to the MN9910 will yield Trise/fall times of 20ns / 30ns.

7. LINEAR vs. PWM DIMMING

The **Linear Dimming** pin is used to control the LED current. There are two cases when it may be necessary to use the Linear Dimming pin.

- ▶ Linear Dimming can be useful to lock-in a desired drive level when the ideal value of RCS is not available..
- ▶ Linear dimming can provide a user dimming function.

To use the internal 250mV, connect the LD pin to VDD.

The only way to fully cut output light is to use the **PWM Dimming** pin. Drive the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off and when the PWMD signal is high, the GATE driver is enabled. Since the PWMD signal does not turn off the other parts of the IC, the response of the MN9910B to the PWMD signal is almost instantaneous. The rate of rise and fall of the LED current is determined by the rise and fall times of the inductor current.

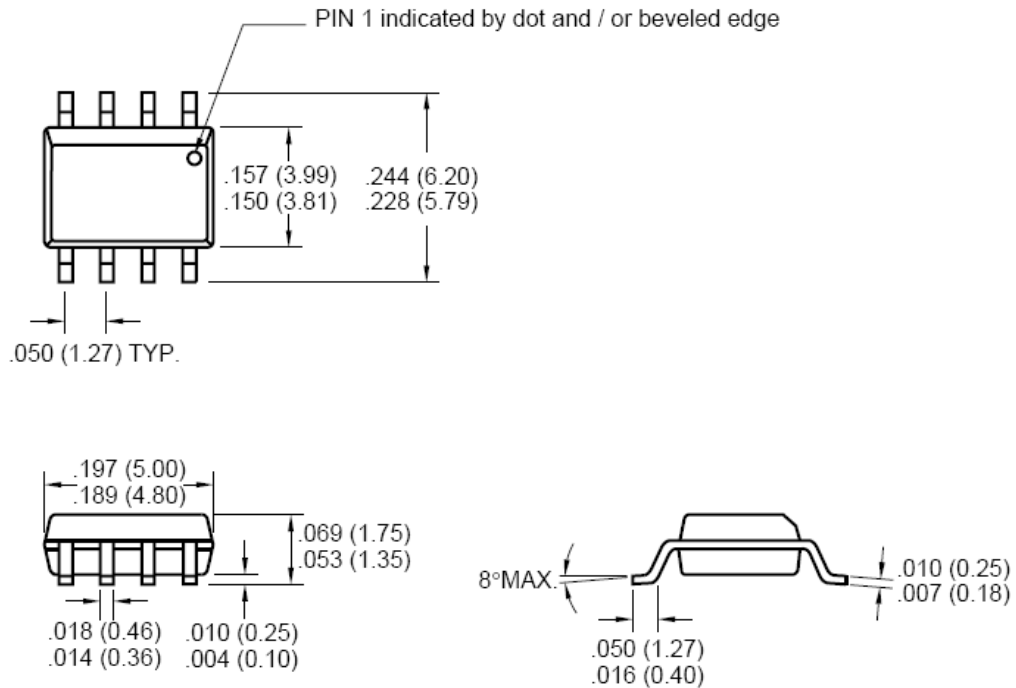
To disable PWM dimming and enable the MN9910B continuous operation, connect the PWMD pin to VDD.

In multi-driver applications, where a particular color balance is desired, PWM dimming maintains the relative drive level of each LED, and thus preserves color balance at all intensities. The disadvantage is that the baseband frequencies associated with the PWM must be kept from spraying into nearby RF modems and Class D amplifiers. Linear dimming is much quieter, but does not preserve color balance across the brightness range. In practical systems, the trim point and temperature compensation for the driver is set with the linear dimming port, while user- dimming is controlled through the PWM port. Care must be then taken to keep the PWM pulse from affecting nearby circuitry.



PACKAGE DIMENSIONS

PLASTIC SOIC-8



NARROW PLASTIC SOIC-16

